

Appl. No. 10/649,067
Amdt. Dated November 14, 2005
Reply to Office Action of June 14, 2005

REMARKS

This is in response to the Office Action mailed June 14, 2005. In the Office Action, Claims 45 and 50 were rejected under 35 U.S.C. § 112, second paragraph; Claims 20-24 and 40-52 were rejected under 35 U.S.C. § 102(b); and the drawings were objected to. Reexamination and reconsideration of this case is respectfully requested in view of the amendments made herein and the following remarks.

Claims 20, 40, 45 and 50 have been amended by this response. Claims 1-19 and 25-39 and were previously cancelled. Claims 53-57 are new claims. Claims 20-24 and 40-57 remain at issue in the patent application. Of those remaining at issue, claims 20, 40, 45, and 50 are independent claims.

Applicant believes that no new matter has been added by this response.

I) OBJECTIONS TO THE DRAWINGS

The drawings were objected to under 37 CFR 1.83(a) as not showing every feature of the invention specified in the claims. The Office Action states that the "storage element" different from a flip flop in claim 50, line 13, and "a selector element" different from a multiplexer in claim 50, line 28 must be shown or the feature(s) cancelled from the claim(s). [Office Action, Page 2].

Applicant has amended claim 50. Applicant believes this objection to the drawings has been overcome in view of the amendments to claim 50 and respectfully requests its withdrawal.

II) CLAIM REJECTIONS UNDER 35 U.S.C. § 112

Claims 45 and 50 were rejected under U.S.C. § 112, second paragraph, as being incomplete for omitting essential structural cooperative relationship of elements, such omission amounting to a gap between the necessary structural connections. [Office Action, page 3].

Applicant has amended independent claims 45 and 50 to clarify the essential structural cooperative relationship of elements. Applicant believes this rejection has been overcome in view of the amendments and respectfully requests its withdrawal.

Appl. No. 10/649,067
Amdt. Dated November 14, 2005
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III) CLAIM REJECTIONS UNDER 35 U.S.C. § 102(b)

Claims 20-24 and 40-52 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,652,904 issued to Trimberger. [Office Action, page 3]. Applicant respectfully traverses.

"To anticipate a claim, the reference must teach every element of the claim. 'A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). ... 'The identical invention must be shown in as complete detail as is contained in the claim.' *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." [MPEP § 2131, 8th Edition, Rev. 1, Feb. 2003, Pg. 2100-701].

Applicant respectfully submits that each and every element as set forth in the claim 20 is not found in Trimberger, nor is the identical invention shown in Trimberger in as complete detail as is contained in amended claim 20.

Amended claim 20 recites in part:

a plurality of multiplexers each having

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•
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an output,

the output coupled to each respective bit of a first bus *coupled to a plurality devices, wherein the first bus is to be kept* in a steady state when inactive. (emphasis added).

The present invention is directed to method and apparatus of bus state keepers for buses in an integrated circuit. By using the bus state keepers 3312, such as those shown in FIG. 33A, the present invention enables power conservation in the integrated circuit. As shown in FIG. 33A, the multiplexer 3308 in the reconfigurable memory controller 2704 outputs to a bus 2716 that is coupled to both the input of a flip flop (register) 3310 and to a device, such as to the memory cluster 2710AA shown in FIG. 27. As described in the detailed description, the selection of the output of flip flop 3310 by the multiplexer 3308 results in the charge on the capacitance of bus 2716 remaining unchanged from its previous state. Keeping bus 2716 in a steady state when inactive to

Appl. No. 10/649,067
Amdt. Dated November 14, 2005
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conserve power. In addition, in response to the select signal, the multiplexer 3308 couples the second bus 2707 to the first bus 2716 and to the memory cluster 2710AA in a transparent manner so that the state of the second bus 2707 can be transferred to the first bus 2716 without any intermediate circuit (such as a flip flop) whose activity is dependent on cycles of a clock.

The Office Action alleges that Fig. 3B of Trimberger discloses the foregoing features of the present invention. [Office Action, Page 3]. Applicant respectfully disagrees. Trimberger does not disclose the foregoing features of the present invention, particularly in regards to a multiplexer that is coupled to each respective bit of a first bus wherein the bus is coupled to a plurality of devices, such as to a flip flop and to a memory cluster, as in the present invention. At the cited reference, Trimberger discloses a multiplexer 121 with a output that only couples to the input of flip flop 122. Trimberger's multiplexer 121 does not couple to any other device, such as to a memory cluster 2710AA as in the present invention. In addition, the activities of Trimberger's flip flop 122 are regulated by a clock signal. Thus even if Trimberger's flip flop 122 were to output to a memory cluster, it would not be a transparent output as in the present invention since it would have to wait for a clock cycle for data to change states.

Moreover, Trimberger's multiplexer 121 is coupled to the flip flop 122 via an internal connection or node that is not a bus. It is well known in the art that a bus is defined as a set of connections to several devices (see definition of "bus" on page 39 in The Harper Collins Dictionary of Electronics by Ian R. Sinclair attached hereto as Exhibit A). The internal connection in Trimberger does not fan out to a plurality of devices and is thus not a bus. Trimberger, as a whole, is thus silent as to the foregoing features of the present invention as claimed in amended claim 1.

The Applicant respectfully submits that because of the foregoing structural and functional differences between Trimberger and the present invention, that each and every element as set forth in the amended independent claim 20 is not found in Trimberger, nor is an identical invention shown in Trimberger in as complete detail as is contained in the amended independent claim 20. Applicant thus respectfully submits that amended independent claims 20 is not anticipated by Trimberger.

Amended independent claims 40, 45 and 50 share in the same above-described novel features of the amended independent claim 20 and for at least the above-stated reasons with regards to amended independent claim 20, Applicant respectfully submits that amended independent claims 40, 45 and 50 are patentably distinguished over the prior art.

Appl. No. 10/649,067
Amdt. Dated November 14, 2005
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Dependent claims 21-24, 41-44, 46-49 and 51-52 directly or indirectly depend from amended independent claims 20, 40, 45 and 50 respectively and thus include all the limitations of their respective independent claims, as well as reciting the above-described further limitations of particular utility. Therefore, for at least the above-stated reasons with regard to amended independent claims 20, 40, 45 and 50, Applicant submits that dependent claims 21-24, 41-44, 46-49 and 51-52 are patentably distinguished over the prior art.

For at least the foregoing reasons, Applicant respectfully requests the Examiner to withdraw the outstanding §102(b) rejection of claims 20-24, and 40-52 by Trimberger.

IV) NEW CLAIMS

Applicant has added new claims 53-54, 55, 56 and 57 that are fully supported by the specification and add no new matter.

New claims 53-54, 55, 56 and 57 depend from amended independent claims 20, 40, 45 and 50, respectively, and therefore are allowable for at least the above-stated reasons in regards to amended independent claims 20, 40, 45 and 50, respectively.

Appl. No. 10/649,067
Amdt. Dated November 14, 2005
Reply to Office Action of June 14, 2005

CONCLUSION

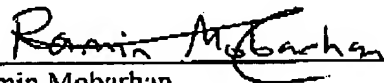
In view of the foregoing it is respectfully submitted that the pending claims are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance of the claims at an early date is solicited.

The Examiner is invited to contact Applicant's undersigned counsel by telephone at (714) 557-3800 to expedite the prosecution of this case should there be any unresolved matters remaining.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such deposit account.

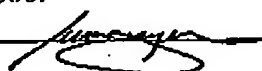
Respectfully submitted,
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Dated: November 14, 2005


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*I hereby certify that this correspondence is
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November 14, 2005 to Examiner Daniel D. Chang at
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Tu Neuven 11/14/2005

Appl. No. 10/649,067
Amdt. Dated November 14, 2005
Reply to Office Action of June 14, 2005

EXHIBIT A

Definition of "Bus"
The Harper Collins Dictionary of Electronics
Ian R. Sinclair
Copyright 1991
Page 39

Appl. No. 10/649,067
Amdt. Dated November 14, 2005
Reply to Office Action of June 14, 2005

THE
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Series Editor, Eugene Ehrlich



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*This book is dedicated to Mrs. Eileen Murphy, whose
husband, Daniel Murphy, was my
colleague and friend for more than 30 years.
Dan's death came shortly after completion
of this, our final collaboration.*

Eugene Ehrlich

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Appl. No. 10/649,067
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BYTE

buncher resonator the electrode of a KLYSTRON that changes the velocity of the electron beam in response to a signal.

buried layer a base layer of high-conductivity SEMICONDUCTOR. The layers of a transistor or integrated circuit are fabricated on top of this buried layer, which then is used for electrical and thermal connections.

burn-in see AGING.

burst a few cycles of signal. See COLOR BURST.

bus 1. a set of connections to several devices. A *power bus* for example, is a set of conductors that carries DC supply to several devices. 2. in computing, a set of lines that connects all the main components such as microprocessor, memory chips, and ports. See also ADDRESS, DATA BUS.

bush a form of bearing or insulator through which a cable shaft is run.

Butterworth filter a filter that produces a flat PASS BAND response, known as a *Butterworth response*, at the expense of steepness in the transition region between pass band and STOP BAND. The amplitude response is given by

$$\frac{V_{out}}{V_{in}} = \frac{1}{[1 + (f/f_c)^{2n}]^{\frac{1}{2}}}$$

where n is the order of the filter, f the frequency, and f_c the cutoff frequency. See also TCHEBYCHEFF FILTER.

by-pass (of a component) providing a shunt for signals. A *by-pass capacitor* for example, shunts unwanted signals to ground.

byte a group of (usually eight) BITS representing a single character.